Claims 1, 2 and 21-26 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,471,373 to Shimizu et al. (Shimizu). Claims 3-9, 13, 14, and 27-42 were rejected under 35 U.S.C. § 103(a) as being obvious over Shimizu. Applicant respectfully traverses these rejections.

The action alleges that Shimizu discloses all the features of a semiconductor integrated circuit device recited in claims 1, 2, and 21-26 relying on Shimizu Figures 1-3 and 18 and a semiconductor substrate (10), transistors Q1, Q2, QE1, QE2, QE3, including gate insulation films of different thicknesses, a terminal for external connection (input/output terminal 5) formed on the substrate, and a transistor QE2 directly connected to the input/output terminal 5 and being a transistor other than the transistor having the thinnest gate insulation film.

Independent claim 1 recites, among other features, that a transistor ***physically connected directly*** to the input/output terminal is one of the transistors other than a transistor having the thinnest gate insulation film. Independent claim 21 recites, among other features, that a transistor connected directly to the input/output terminal, ***absent any intervening elements***, is one of the transistors other than a transistor having the thinnest gate insulation film.

The Action alleges that the transistor QE2 (in FIG. 18 of Shimizu) shows a transistor physically connected directly to the input/output terminal 5 (of Fig. 1) as recited in the claim 1 invention. Also, the action alleges that QE2 is a transistor connected directly to the input/output terminal 5, absent any intervening elements as called for in claim 21. According to FIG. 18 and the corresponding description at column 6, line 66 to column 7, line 10 of Shimizu, the transistor

QE2 is used for the writing operation, and is connected with an interconnection layer 31. However, the specification is devoid of a teaching as to how the transistor QE2 or the interconnection layer 31 is connected to the input/output terminal 5 directly or otherwise. Consequently, Shimizu lacks a teaching or suggestion that the transistor QE2 is *physically connected directly* to the input/output terminal 5 as called for in claim 1 and that the transistor QE2 is connected directly to the input/output terminal 5, ***absent any intervening elements***. In the event, the Examiner maintains the above rejection, applicant respectfully requests the Examiner to identify where (column and row) in the description of Shimizu the claimed structural relations can be found.

Applicant also submits that the such teachings are not inherent from Shimizu. The fact that the transistor may be connected in such a manner is not sufficient to establish inherency. It must necessarily be connected in such a manner. Significantly, applicant has recognized an advantage with the structures recited in claims 1 and 21 in that a plurality of transistors based on gate oxide films of two or more different thicknesses can be integrated within one chip without deterioration in the transistor characteristics, and the breakdown voltage against ESD can be reduced.

In light of the foregoing, Shimizu lacks a teaching of all the features recited in independent claims 1 and 21. Also, claims 3-9, 13 and 14, which ultimately depend from claim 1, and claims 22-31, which ultimately depend from claim 21, are patentably distinct for the same reasons as their ultimate base claim, and further in view of the additional advantageous features recited therein.

Independent claim 32 calls for, among other features, that a transistor *always connected directly* to the input/output terminal is one of the transistors other than a transistor having the thinnest gate insulation film. Apparently, the action recognizes that Shimizu does not disclose all the features recited in claim 32 since this claim has been rejected as being obvious. In this regard, applicants note that the only difference between claim 32 and claim 1 is that claim 32 uses the word *always* rather than "physically" to describe the direct connection between the transistor and the input/output terminal. Indeed, the action states that "Shimizu discloses the use of thin gate oxide transistors for the 'read' operation of an EPROM device and thick gate oxide transistors used for the 'write' operation, as well as other peripheral circuits." Thus, the action admits that a gate oxide transistor (e.g., QE2) is connected to the input/output terminal 5 during the write operation, and not the read operation. See also, col. 7, ll. 7-8. Stated otherwise, the action acknowledges that Shimizu fails to teach or suggest that a transistor *always connected directly* to the input/output terminal is one of the transistors other than a transistor having the thinnest gate insulation film as required by claim 32. The action fails to overcome this deficiency and identify any suggestion in Shimizu to modify the transistor QE2 to be *always* connected to the input/output terminal 5.

Claims 33-42, which ultimately depend from claim 32, are allowable for the same reasons as their ultimate base claim, and further in view of the additional advantageous features recited therein.

CONCLUSION

In light of the foregoing, applicant respectfully submits that the instant application is in condition for allowance, and solicits prompt notification of the same.

Respectfully submitted,

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